UNITED STATES PATENT APPLICATION

FOR

SYSTEM FOR SUBSTRATE POTENTIAL REGULATION DURING POWER-UP IN INTEGRATED CIRCUITS

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SYSTEM FOR SUBSTRATE POTENTIAL REGULATION DURING POWER-UP IN INTEGRATED CIRCUITS

FIELD OF THE INVENTION

Embodiments of the present invention relate to circuits for providing operational voltages in complementary metal-oxide semiconductor (CMOS) circuits. In particular, embodiments of the present invention relate to a charge pump circuit with a variable output.

BACKGROUND ART

As the operating voltages for CMOS transistor circuits have decreased, variations in the threshold voltages for the transistors have become more significant. Although low operating voltages offer the potential for reduced power consumption, threshold voltage variations due to process and environmental variables often prevent optimum efficiency and performance from being achieved due to increased leakage currents.

Prior Art FIG. 1 shows a conventional CMOS inverter 100. A P-type substrate 105 supports an NFET 110 and a PFET 120. The NFET 110 comprises a gate 112, source 113, and drain 114. The PFET 120 resides in an n-well 115, and comprises a gate

122, drain 123, and a source 124. The substrate 105 and source 113 are coupled by a tie 130 that is connected to ground (GND), while source 124 and N-well 115 are coupled by a tie 135 that is connected to a supply voltage (V_{DD}). The input to the inverter is applied to the gates 112 and 122, with the output taken from the drain contact 125. In this conventional configuration, the transistors are often treated as three terminal devices.

Threshold voltage variations may be compensated for by body-biasing. Body-biasing introduces a reverse bias potential between the bulk and the source of the transistor that allows the threshold voltage of the transistor to be adjusted electrically. The purpose of body-biasing is to compensate for 1) process variations; 2) temperature variations; 3) supply voltage variations; 4) changes in frequency of operation; and 5) changing levels of switching activity.

Prior Art FIG. 2 shows an inverter having connections for body-biasing. Body-bias can provided to the PFET 120 through a direct bias contact 150a, or by a buried n-well 140 using contact 150b. Similarly, body-bias may be provided to the NFET 110 by a surface contact 155a, or by a backside

contact 155b. An aperture 145 may be provided in the buried n-well 125 so that the bias potential reaches the NFET 110. In general, a PFET 120 or an NFET 110 may be biased by one of the alternative contacts shown.

In integrated circuits that employ body-biasing, the transistors are effectively four terminal devices, and the substrate potential is not be maintained at ground. When the substrate bias supply (e.g., V_{BBP}) is off the substrate potential may float.

A floating substrate potential can be a problem during the initial application of power to an integrated circuit. When a body-bias (e.g., V_{BBN}) is initially applied to an N-well, leakage to the substrate from that N-well may cause the substrate potential to rise. This rise in substrate potential can forward bias the junction between the substrate and N-wells that are not connected to V_{BBN}, causing undesired current flow.

SUMMARY OF INVENTION

Thus, a need exists for a system for preventing undesired current flow during power-up in integrated circuits that employ body-biasing.

Accordingly, embodiments of the present invention provide a switch or clamp that responds to conditions at power-up and prevents a circuit substrate from floating.

In one embodiment of the present invention, a bias input (V_{BBN}) to an N-well is coupled to a control input for a single-pole, double-throw switch that couples an integrated circuit substrate to ground or to a bias voltage supply (V_{BBP}). When V_{BBN} is on and V_{BBP} is off, the switch couples the substrate to ground. When V_{BBP} is on, the switch couples the substrate to V_{BBP}.

In another embodiment of the present invention, a bias input (V_{BBN}) to an N-well is coupled to a control input for a single-pole, double-throw switch. The switch also has a control input coupled to a charge pump enable signal line (CP_{ENABLE}). When V_{BBN} is high and CP_{ENABLE} is low, the switch couples the substrate to ground. CP_{ENABLE} is high, the switch is open.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

Prior Art FIG. 1 shows a conventional CMOS inverter without body-bias connections.

Prior Art FIG. 2 shows a conventional CMOS inverter with body-bias connections.

FIG. 3 shows a diagram of a portion of an integrated circuit with body-bias inputs coordinated by a single-pole, double throw (SPDT) switch, in accordance with an embodiment of the present claimed invention.

FIG. 4 shows a diagram of a portion of an integrated circuit with body-bias inputs coordinated by a single-pole, single-throw (SPST) switch, in accordance with an embodiment of the present claimed invention.

FIG. 5 shows a timing diagram for the body-bias potentials on power-up, in accordance with an embodiment of the present claimed invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the present invention, a variable output charge pump circuit, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuit elements have not been described in detail as not to unnecessarily obscure aspects of the present invention.

FIG. 3 shows a diagram 300 of a portion of an integrated circuit with a P-type substrate 305 having a first N-well 310 and a second N-well 315. Body-bias V_{BBN1} is provided to N-well 310 and body-bias V_{BBN2} is provided to N-well 315. Body-bias V_{BBN1} is coupled to switch 320 as a control input 321, and body-bias V_{BBN2} is optionally coupled to switch 320 as a control input 322. The switch 320 has a switched terminal coupled to V_{BBP} and a switched terminal coupled to ground. The switch has a fixed output terminal coupled to the substrate. As used herein, the term "coupled" refers to a physical coupling and does not necessarily imply an electrical

coupling. Electrical coupling may made selectively between elements that are physically coupled.

Switch 320 acts as a single-pole, double-throw (SPDT) switch, selectively and electrically coupling the substrate 305 to body bias V_{BBP} or ground, depending upon the state of bias supply lines V_{BBN1}, V_{BBN2}, and V_{BBP}. If V_{BBN1} (or V_{BBN2} if present) is high and V_{BBP} is off, the switch 320 electrically couples the substrate 305 to ground. By electrically coupling the substrate to ground, the switch prevents the substrate from floating up to a potential that could forward bias the junction between the substrate and an unbiased N-well in the integrated circuit.

Operating power is supplied to the switch 320 by a small auxiliary charge pump (not shown) rather one of the bias lines, since it is desirable that the switch be able to operate regardless of the state of the bias lines.

If V_{BBP} is on (e.g., -1.2 volts) and V_{BBN1} (or V_{BBN2} if present) is high, the switch 320 couples the substrate to V_{BBP}. For the case when V_{BBP} is on while V_{BBN1} and V_{BBN2} are low, the switch may be built to switch the substrate to either V_{BBP} or to ground, depending upon other design considerations. For all possible bias input combinations, the switch 320 provides

a regulated substrate potential that prevents undesirable forward biasing of the substrate/N-well junction.

For all possible bias input combinations, the switch 320 provides a regulated substrate potential that prevents undesirable forward biasing of the substrate/N-well junction. The switch operates to electrically couple the substrate to a substrate bias voltage or to ground, in response to particular combinations of bias voltages on the N-well and substrate bias lines.

FIG. 4 shows a diagram 400 of a portion of an integrated circuit with a P-type substrate 305 having a first N-well 310 and a second N-well 315. Body-bias V_{BBN1} is provided to N-well 310 and body-bias V_{BBN2} is provided to N-well 315. Body-bias V_{BBN1} is coupled to switch 405 as a control input 406, and body-bias V_{BBN2} is optionally coupled to switch 405 as a control input 407.

A charge pump 410 having a V_{BBP} enable input is coupled to substrate 305. The V_{BBP} enable input is also coupled to the switch 405 as a control input 408. The charge pump 410 provides the bias potential V_{BBP} for the substrate 305.

Switch 405 acts as a single-pole, double-throw (SPDT) switch, coupling the substrate 305 to ground, depending upon the state of V_{BBN1}, V_{BBN2}, and V_{BBP} enable. If V_{BBN1} (or V_{BBN2} if present) is high and V_{BBP} enable is low, the switch 405 couples the substrate 305 to ground. By clamping the substrate to ground, the switch prevents the substrate from floating up to a potential that could forward bias the junction between the substrate and an unbiased N-well in the integrated circuit.

If V_{BBP} enable is high and V_{BBN1} (or V_{BBN2} if present) is high, the switch 405 isolates the substrate from ground. It is desirable that the switch 405 be sufficiently fast to isolate the substrate before the charge pump output reaches a significant value. In general, a charge pump turn-on will be slower than that of the switch 405.

FIG. 5 shows a representative timing diagram 500 for the body-bias, N-well, and substrate potentials on power-up, in accordance with an embodiment of the present invention. Trace 505 shows the turn-on or enablement of the N-well bias supply V_{BBN1}. The sharp edge is idealized, and corresponds to a logic signal initiating the application of V_{BBN1}.

Trace 510 shows the voltage of the N-well rising from ground (GND) to V_{BBN1} over time as the capacitance associated junction between the substrate and well is charged. Since bias supplies typically have a low current demand under steady state conditions, the initial rise time is slower than that of trace 505 due to the limited current.

Trace 515 shows the turn-on or enablement of the P-type substrate bias supply V_{BBP}. The sharp edge is idealized, and corresponds to a logic signal initiating the application of V_{BBP} (e.g., the signal V_{BBP} enable of FIG. 4). Trace 510 shows the voltage of the P-type substrate dropping from ground (GND) to V_{BBP} over time as the capacitance associated junction between the substrate and well is discharged. Since bias supplies typically have a low current demand under steady state conditions, the initial rise time is slower than that of trace 515 due to the limited current.

As shown by trace 520, the action of the substrate regulating switch of the present invention prevents the substrate potential from rising above ground. The substrate potential is maintained between ground and V_{BBP}.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of

illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. For example, an integrated circuit having a P-type substrate and an N-well disposed therein is described. More generally, the invention may be used with a semiconductor substrate of either N-type or P-type having a complementary well disposed therein. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.